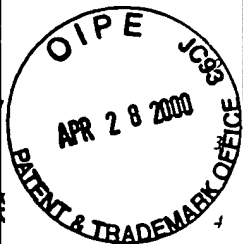


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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Application Serial No. .... 09/420,635  
Filing Date .... October 21, 1999  
Inventor .... Werner Juengling  
Assignee .... Micron Technology, Inc.  
Group Art Unit .... 1746  
Examiner .... Unknown  
Attorney's Docket No. .... MI22-1243  
Title: Semiconductor Processing Methods of Forming Devices on a Substrate,  
Forming Device Arrays on a Substrate, Forming Conductive Lines on a  
Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated  
Circuitry

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed  
to the United States patents and other references listed on the attached Form PTO-  
1449. No admission is made regarding whether all the submitted references are prior  
art.

This Supplemental Information Disclosure Statement is being filed within three  
months of the filing date of the application or before the mailing of a first Office  
Action, whichever occurs last. Therefore, no fee is believed to be required. However,  
in the event that a fee is required for filing this Supplemental Information Disclosure  
Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account  
No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the  
above fee.

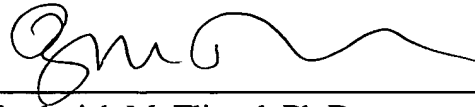
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TC 700 MAIL ROOM

1 Citation of these references is respectfully requested.

2 Respectfully submitted,

3  
4 Date: April 25, 2000



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